PARALLEL PROCESSOR ARRAY FOR HIGH SPEED PATH PLANNING

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ABSTRACT

The first integration of a 24 x 25 array of processors for high speed optimal path planning is reported. Based on programmed terrain costs (traversal time), the IC determines, in parallel, the fastest routes from a selected starting point(s) to all other points on a given terrain. The chip has been successfully tested at a 7 MHz clock frequency, with typical path determination requiring 230 μs, resulting in a four order of magnitude speed-up over current software-based shortest-route techniques.

INTRODUCTION

For a given terrain to be traversed, it is computationally intensive to determine the fastest route between two points, and for defense or civilian emergency dispatching applications, computation time is critical. This paper reports the integration of a 24 x 25 random access array of digital processors which are programmed to model a given terrain and determine the fastest (lowest cost) path between any points on the terrain at very high speed (milliseconds for arrays up to 512 x 512). The primary purpose of this research chip is to demonstrate high speed path planning capability for tactical mobility analysis in battlefield scenarios. However such high speed automated path planning will find utility in a variety of settings such as autonomous vehicle navigation, intelligent vehicle highway systems, evacuation and rescue planning, and police and transportation dispatching.

Currently, the only tools available to assist in path planning are implemented in software. These approaches can be slow, with best path determination typically requiring seconds to minutes for terrain sizes varying from 64 x 64 to 512 x 512 pixels.[1] Through the VLSI implementation of a fine grain parallel architecture, in which every terrain pixel is represented by a corresponding processor, the inherent parallelism of the problem can be exploited and extremely fast path determination can be realized. In such an architecture, the only processor communication required is between nearest neighbors so that processor communication overhead is virtually eliminated. This is in contrast to conventional parallel computers, where even with proper parallel decomposition of the problem, processor communication overhead is often a severe speed bottleneck. In this paper, the first parallel processor IC for route planning over complex terrain is reported.

ARRAY ARCHITECTURE AND OPERATION

The path planner architecture, shown schematically in Fig. 1, consists of a 24 x 25 array of unit cells (processors) which communicate with their nearest neighbors and are randomly accessed by 5-bit row and column decoders located adjacent to the array. The IC is implemented in a single-poly, double-metal 2 μm CMOS n-well process, utilizing a full custom layout. The overall chip area is 9.2 mm x 7.9 mm. A photograph of the chip is shown in Fig. 2.

In order to determine the fastest routes from a selected starting point(s) to all other points on a given terrain, each unit cell corresponds to a terrain pixel which has been preprogrammed with the cost (i.e. delay) of traversing that pixel. Operation begins with the selection of a path origination pixel(s) which sends out a signal to its north, south, east and

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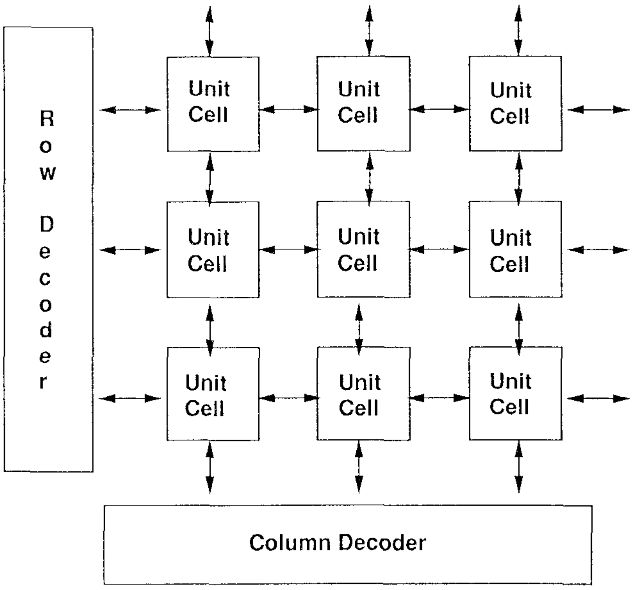


Fig. 1 Block diagram of IC architecture.

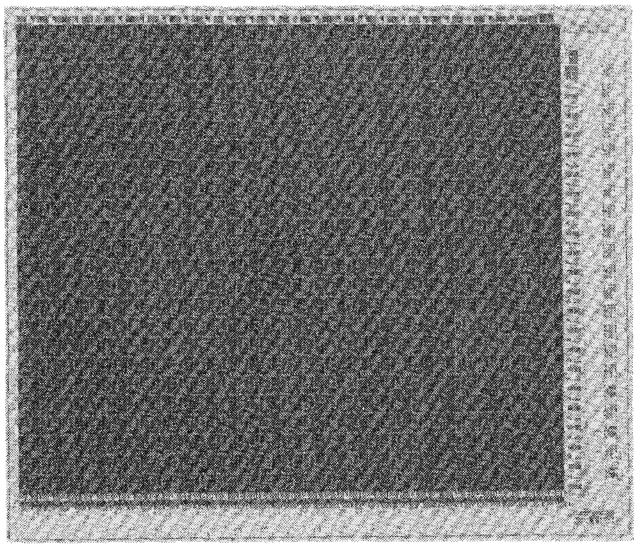


Fig. 2 IC photograph.

west neighbors. Each neighbor delays the signal by a preset time (programmable cost), after which it broadcasts a signal to each of its four neighbors. One of 256 costs (delays) can be selected. When a signal is received, the incoming signal direction is stored and further inputs to the cell are disabled. This results in a signal wavefront propagating radially outward from the originating pixel that is then distorted by the varying delays encountered in the array. When signal propagation through the entire array is complete, any destination node may be queried and the minimum path between it and the origination node is found by retracing the direction stored in each unit cell. Thus, determination of the fastest paths through a complex terrain (modelled by 256 cost levels) is realized. This is in contrast to the simpler task of maze solving or wire routing, in which the processors would be programmed with binary costs, i.e. the pixel is either blocked or open. A 4 x 4 array of such binary processors and later a 4 x 8 array which used the discharge of a capacitor to provide an additional cost (blocked, not blocked and slow) have been previously reported.[2] In addition to the lack of available cost levels, another drawback of this approach is the uncontrolled cost nonuniformity associated with varying capacitor discharge times across the array. In the approach reported here, the all-digital implementation leads to perfect cost uniformity across the array.

In addition to finding the fastest paths from one origination pixel to all possible destinations, multiple starting pixels can be selected, with signal propagation emanating from each source and stopping at the boundary between signal wavefronts. This feature is useful in battlefield scenarios where an analyst can model the progress of different forces across the terrain. In addition, when any destination node is queried, the minimum path between it and the nearest source pixel is displayed, which provides valuable information for rescue operations.

Unit Cell

In order to implement signal propagation and path retracing in the array, each unit cell must perform two main functions: programmable delay and storage of the incoming direction. The former is implemented with a programmable counter and the latter with a set of static latches. A block diagram of the unit cell is shown in Fig. 3 and occupies 296 µm x 330 µm. Signal propagation through the array, controlled by variable unit cell delays, is implemented by presetting an 8-bit ripple down-counter in each cell to one of its 256 possible values. When triggered by an incoming signal the counter decrements down to zero that in turn triggers the broadcast of an outgoing signal to each of its nearest neighbors.

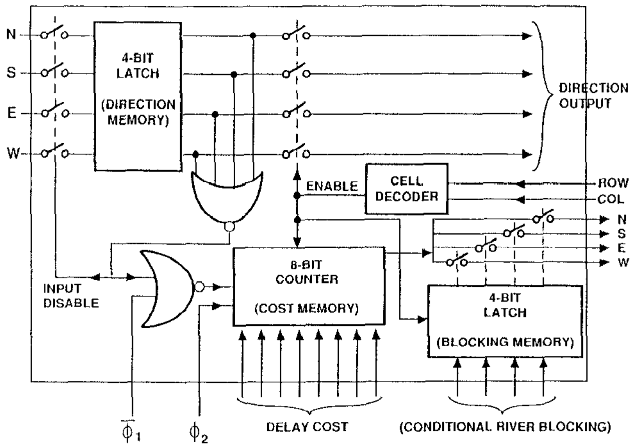


Fig. 3 Block diagram of unit cell processor.

Each counter stage is based on a static latch configuration, shown in Fig. 4. To eliminate the need for an 8-input NAND gate, nine (rather than eight) counter stages are utilized to achieve the 256 delay resolution. In order to implement the path retracing function in the array, four static cross-coupled latches are used to store the incoming signal direction. They can be read out at any time, even during signal propagation through the array. A four input NOR gate is triggered if any of the latches are set, that in turn disables the static latches from receiving further input.

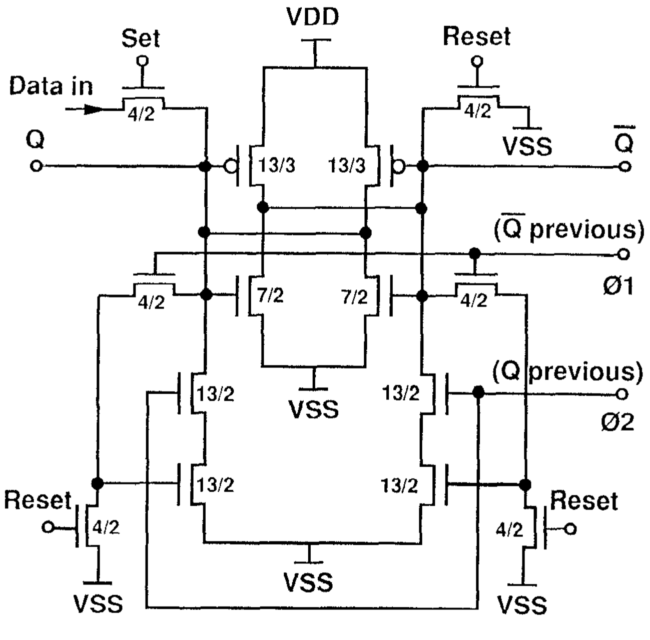


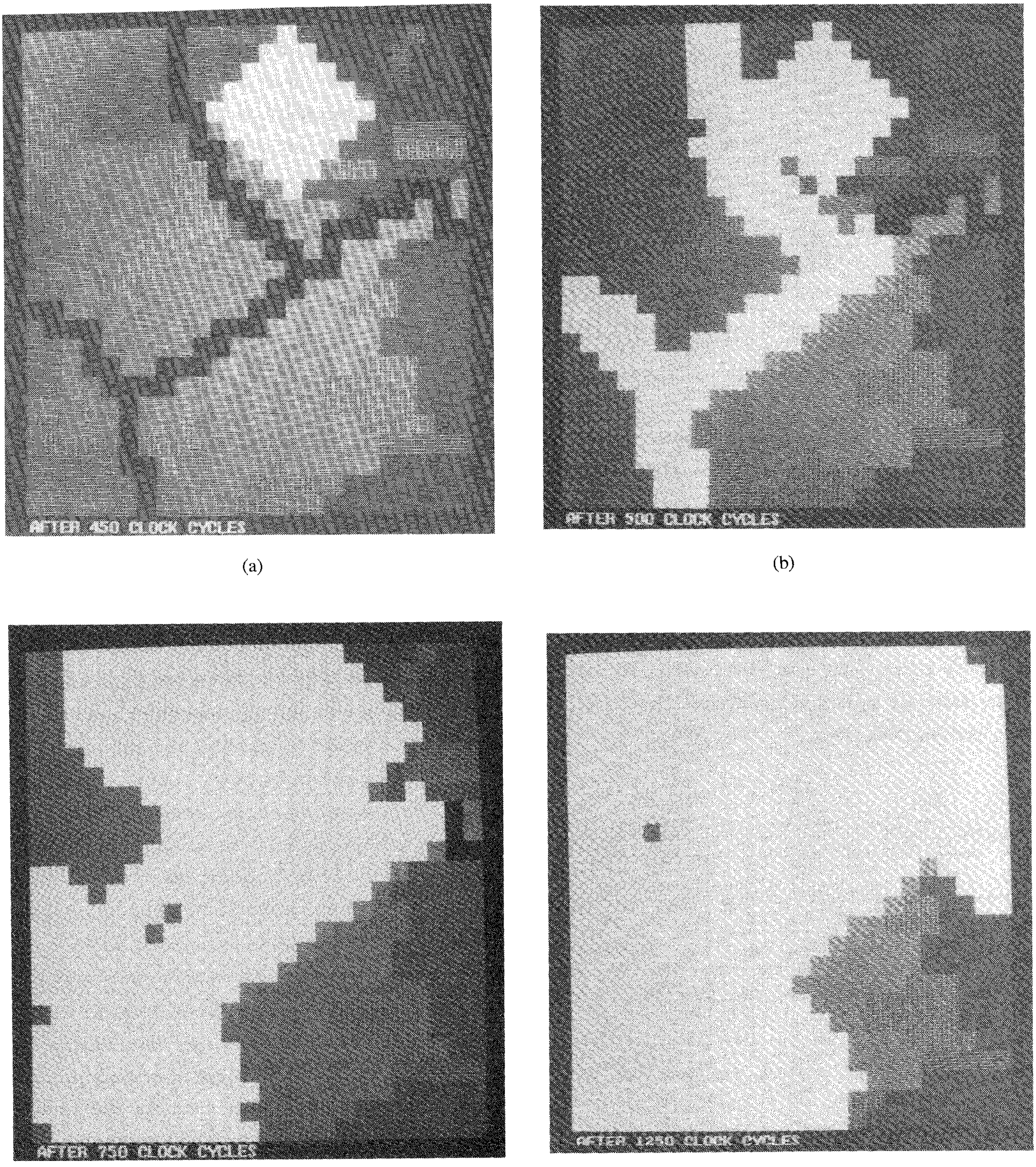
Fig. 4 Circuit schematic of one counter stage.

Another unit cell function is the conditional blocking of signal propagation in any direction to model impassable terrain such as rivers and canyons. This is important because the current (and next generation) resolution of digitized map data results in single pixels which contain both rivers and other features such as roads. In this case, the unit cell is assigned the cost of a road and the outgoing signal is blocked from crossing the river, resulting in signal propagation along a road adjacent to a river. Such conditional blocking is accomplished with another set of four static latches which are preprogrammed to either block or transmit the signal emanating from the counter.

In order to minimize the unit cell size, each of the three functional blocks (storage of incoming direction, programmable delay, and conditional signal blocking) access four common data lines when enabled. The enable circuitry and row/column decoder found in each unit cell are implemented primarily with NOR logic.

EXPERIMENTAL RESULTS

The path planner chip was interfaced to a laboratory PC computer through a wirewrap board and plug-in digital interface card. The entire chip (address memory, counter, river blocking, control logic and I/O) is completely functional. It was found that the latches require 160 ns to settle, implying a terrain programming time for the 600 pixel array of less than 300 µs. A separate counter test circuit was successfully clocked at 8.33 MHz, limited by the test station. The array can be operated in two modes: single step and continuous. In the former, the chip is clocked via the PC, and the actual signal propagation on the chip can be monitored on the PC screen. An example of signal propagation through the array is given by the sequence of photos in Fig. 5. In the continuous mode, a function generator supplies a square wave input to an nonoverlapping clock generator located on the wire-wrap board which in turn clocks the counter. The chip was tested at frequencies up to 7 MHz in this mode, resulting in typical path determination times of under 250 µs. For a typical terrain cost map, signal propagation through the array required 2550 clock cycles, so that the entire signal propagation phase required only 360 µs at a 7 MHz clock rate. Fig. 6 displays the original map with a typical lowest cost path shown in white.



(a)

(b)

(c)

(d)

Fig. 5 Signal propagation through array shown in white on map background (black indicates road): a) after 450 clock cycles, b) after 500 clock cycles, c) after 750 clock cycles, and d) after 1250 clock cycles.

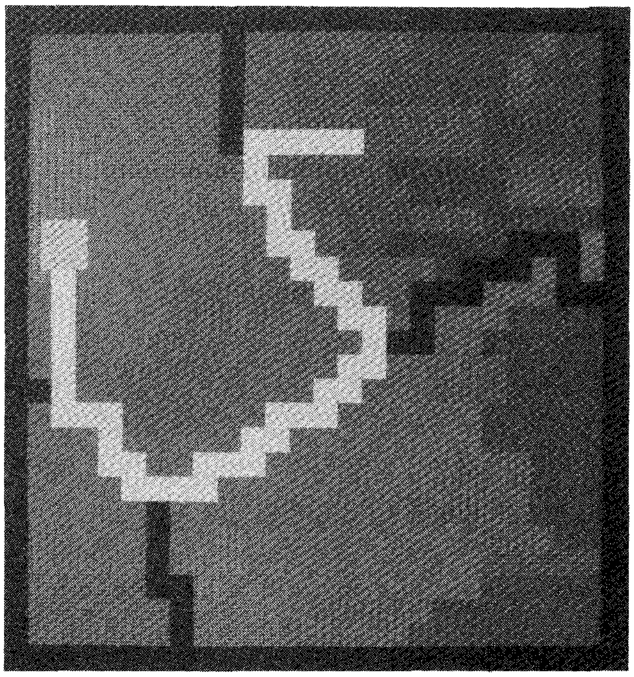


Fig. 6 A typical lowest cost path found by chip.

CONCLUSION

In summary, the first single-chip fine grain parallel processor array to perform path planning over complex terrain has been demonstrated. The 24 x 25 array of digital processors has been operated at frequencies up to 7 MHz, providing best (fastest) route determination in under a millisecond. This corresponds to a four order of magnitude speed-up over current software approaches. Full functionality of this first generation research chip paves the way for the implementation of large arrays (e.g. 1024 x 1024) and chips with increased functionality. Both these avenues are currently being pursued. A summary of the chip characteristics is given in Table 1.

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Table I IC Characteristics

Chip Architecture:	24 x 25 digital processor array
Maximum Clock Frequency:	7 MHz
Equivalent Operations per second:	6 billion
Origination Nodes:	one or multiple
Cost Dynamic Range:	256:1
Process:	2 μm CMOS
Unit Cell (Processor) Size:	296 μm x 330 μm
IC Size:	7.9 mm x 9.2 mm

REFERENCES

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